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L1	425	(717/128).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/16 15:35
L2	507753	blocking	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/16 15:35
L3	29	1 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/16 15:35

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1   Blocking: exploiting spatial locality for trace compaction   ■

Anant Agarwal, Minor Huffman
April 1990 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1990 ACM SIGMETRICS conference on Measurement and modeling of computer systems SIGMETRICS '90**, Volume 18 Issue 1
Publisher: ACM Press

Full text available: pdf(1.01 MB)   Additional Information: full citation, abstract, references, citings, index terms

Trace-driven simulation is a popular method of estimating the performance of cache memories, translation lookaside buffers, and paging schemes. Because the cost of trace-driven simulation is directly proportional to trace length, reducing the number of references in the trace significantly impacts simulation time. This paper concentrates on trace driven simulation for cache miss rate analysis. Previous schemes, such as cache filtering, exploited temporal locality for compressing traces and ...

2   The block-based trace cache   ■

Bryan Black, Bohuslav Rychlik, John Paul Shen
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture ISCA '99**, Volume 27 Issue 2
Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(181.08 KB)   Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

The trace cache is a recently proposed solution to achieving high instruction fetch bandwidth by buffering and reusing dynamic instruction traces. This work presents a new block-based trace cache implementation that can achieve higher IPC performance with more efficient storage of traces. Instead of explicitly storing instructions of a trace, pointers to blocks constituting a trace are stored in a much smaller trace table. The block-based trace cache renames fetch addresses at the basic block le ...

3   Completion time multiple branch prediction for enhancing trace cache performance   ■

Ryan Rakvic, Bryan Black, John Paul Shen
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture ISCA '00**, Volume 28 Issue 2
Publisher: ACM Press

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